REMARKS

Under 35 USC § 102(b), claims 1-3, 6-7, 9-12, 14, and 17-20 were rejected as anticipated by Pua et al (US Pat. App. No. 20020147882A1). Claim 8 was rejected under 35 USC § 103(a) as obvious over Pua in view of common knowledge to one of ordinary skill in the art at the time of Applicant's invention. Claim 15 was rejected under 35 USC § 103(a) as obvious over Pua further in view of IEEE1394 Standard. Claim 16 was rejected under 35 USC § 103(a) as obvious over Applicant's admitted prior art (AAPA) and further in view of Pua.

Claims 4-5, 13, and 21 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The limitations of allowable claim 13 are being incorporated into base claim 10, and claims 11-13 are being canceled. Thus amended claim 10 should be allowable.

Female USB Connector is Missing

For claim 1, Pua's extension stack connector 20 was cited as the claimed female USB connector, while Pua's USB connector 10 was cited as the claimed male USB connector. However, Pua shows that his extension stack connector is not a USB connector. Indeed, nowhere does Pua teach or even suggest that his connector 20 is a female USB connector that can fit into a male connector such as his USB connector 10. Thus Pua lacks a female USB connector as recited in claim 1.

Pua's Connector 20 Has Chip-Select Pins, So Cannot be USB

Indeed, Pua's connector 20 does not appear to be a USB connector at all. Applicant's specification describes the four signals in a USB connector:

> Connector 38 is a USB connector with metal contacts for the standard power, ground, and differential data D+, D- lines. (Spec. para [005]).

Pua describes "pins" in his connector 20 that are needed by the flash-memory chip:

> The extension stack connector connects the pins needed by the flash memory chip on the slave board with the controller on the main board. (Pua Para. [0012]).

Since it is well known that a flash memory chip has more pins than the 2 data and 2 power/ground pins in a USB interface, Pua's connector 20 cannot be a USB connector. Indeed, Pua describes multiple chip-select pins:

> [0045] The device can support more than one piece of flash memory. In the present invention, multiple chip select pins are provided. When the device is initialized, it will check the type of the flash (the capacity) being used on board and how many chips the system has and the device will add up all the memory chips to find out the total capacity. When the host needs this kind of data, the device will provide the total capacity to the host, not just the capacity of one chip.

Since chip-select is not a signal in the USB connector, Pua's connector 20 to the flash-memory chips cannot be a USB connector since the "multiple chip-select pins" to the flash-memory chips 120 on slave boards 150 are connected through connectors 20, 110.

Pua's Connector 20 Cannot Fit into Pua's USB Connector 10

Extension stack connector 20 was cited as the claimed female USB connector, while USB connector 10 was cited as the claimed male USB connector. Claim 3 recites that the "female USB connector can connect to the male USB connector of a downstream chainable USB flash-memory drive ". Nowhere does Pua teach or even suggest that his extension stack connector 20 can plug into his USB connector 10. Indeed, Pua suggests that these two connectors have different sizes and are thus not compatible. Pua's Fig. 1A shows that USB connector 10 is short and wide (long), while extension stack connector 20 is tall and narrow.

Indeed, there are two extension stack connectors 20 on the board, and it appears that Pua's expansion board 150 of Fig. 1B fits over both of these, since there are also two matching connectors 110 on board 150 of Fig. 1B that are the same shape and size as extension stack connectors 20 of Fig. 1A. Perhaps these are called "stack" connectors because the expansion boards might be stacked over one another, sandwich-style.

Since Pua explicitly shows different shapes and sizes for his connectors 10, 20, and nowhere teaches that connector 20 plugs into connector 10, Pua cannot render claim 3 obvious. Indeed, it is more likely that Pua teaches away, since his connector 20 is the

same shape and size as his connector 110, rather than his USB connector 10 and Pua explicitly teaches that board 150 (Fig. 1A) connects to board 100 (Fig. 1B):

> [0073] The main board 100 of the flash memory device 5 can also have a stack connector 20 for connecting a slave board 150 to the main board 100 for extending the memory size with additional flash memory 120. The slave board 150 comprises at least one additional flash memory array or module 120. Multiple slave boards can be connected in order to provide unlimited memory expansion.

Pua Missing a Pass-Through to Second USB Connector

Claim 17 recites:

> pass-through means for passing the protocol data from the host through to the female protocol connector means when the host addresses a port that is not in the plurality of ports of the protocol hub controller means,

Pua teaches that USB protocol data is received from the host:

> [0076] The controller 200 of the flash memory device of the present invention performs numerous functions. Among these functions is controlling the USB interface 210.
>
> [0077] The controller 200 follows the USB specification for physical and logical protocol. The controller 200 further comprises a system buffer 250 or FIFO controller buffer.
>
> [0078] The controller 200 receives command and parameter packets from the USB host, which are then stored in the system buffer 250 defined by the controller 200. The controller 200 is also responsible for controlling the transfer of data to and from the USB host.
>
> [0079] In addition, the controller 200 also provides status data to the USB host.

This USB protocol data is transferred between the host and a 512- byte buffer (250 of Fig. 2) using a USB engine:

> [0142] When the device executes a read command, the controller will first read data from the flash memory, sector by sector to a buffer (512 bytes) in the controller, then this sector will be sent to the host by a USB engine. The whole command will be completed when the number of sectors that have been sent to the host is equal to the sector count.
>
> [0143] When the device executes a write command, the controller will read data from the host by the USB engine sector by sector to a buffer (512 bytes) in the controller, and then this sector will be stored in the flash memory. The whole command will be completed when the number of sectors that have been sent to the flash memory is equal to the sector count.

Thus Pua teaches that his 512-byte buffer acts as a protocol endpoint. The USB interface 210 is separate from the flash-memory interface 250 in Fig. 2:

> [0085] A system buffer 250 is used as a cache which is provided for buffering between the **USB interface 210** and the **flash memory array interface 260**. It is also the FIFO of the USB protocol and the direction map to the buffer. The microprocessor 220 manages the addresses of this buffer. As required, the buffer can be accessed by byte or word. (emphasis added)

Pua lacks any pass-through means that passes protocol data from the host to his extension stack connector 20, which was cited as the claimed female protocol connector means.

Pua's "flash memory array interface 260" is complex. Pua's flowcharts of Figs. 6, 7 shows write and read procedures that are executed over the flash-memory interface in response to write and read USB commands. In particular, the USB logical address is converted to a physical address for the flash-memory interface. See paragraphs [0118] and [0132].

Pua's paragraph [0145] was cited as teaching the pass-through means:

> [0145] When the host sends a certain address (logic) to the device, the device will perform a calculation to find the exact chip and corresponding address that the host wants to access. Then the calculated address is used and the chip select pin is enabled.

However, this paragraph teaches that the host's address is changed into a calculated address that is used. Also, this paragraph teaches that a chip-select pin is enabled. The USB protocol does not have a chip-select pin. Thus Pua is teaching away from passing-though protocol data, since Pua teaches that his USB protocol address is changed, and that a chip-select pin to the flash is used for a flash-memory interface that is not the USB interface. There is no pass-through of USB data in Pua.

In view of the above, it is submitted that claims 1-9, 11-21, as amended, are in a position for allowance. This application was filed with formal drawings that have not been amended. Applicant believes that a full and complete response to the office action has been made. Reconsideration and re-examination is respectfully requested. Allowance of the claims at an early date is solicited.

If the Examiner believes that a telephone interview would expedite prosecution of this application, he is invited to telephone the undersigned at (831) 476-5506.

Respectfully Submitted,

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